Changes Required for PCIe 5.0 by Chapter

Chapter 1 - Introduction

No changes are anticipated for the material in this chapter.

Chapter 2 – Transaction Layer Specification

No changes are anticipated for the material associated with the following areas.

- The number of available tags are adequate for 32.0 GT/s and no changes are anticipated.
- Scaled flow control is adequate for 32.0 GT/s and no changes are anticipated.

Changes will be made for the material associated with the following areas.

- A table for 32.0 GT/s will be added to Sec 2.6 Flow Control - Table 2-49a: Maximum UpdateFC Transmission Latency Guidelines for 32.0 GT/s (Symbol Times) - likely table 2-50

Aside from the above, no other changes are anticipated for the material in this chapter.

Chapter 3 – Data Link Layer Specification

Aside from the following, no other changes are anticipated for the material in this chapter.

- The Replay Timer text will need to be tweaked.
- A table will be added in section 3.6.2.1 (Maximum Ack Latency Limits for 32.0 GT/s (Symbol Times) – also the other tables will be reviewed

Chapter 4 – Physical Layer Logical Block

No changes are anticipated for the material associated with the following areas.

- The Physical Layer will follow the 128b/130b encoding when operating at the 32.0 GT/s Data Rate.
- Lane Margining at Receiver is expected to remain unchanged at the 32.0 GT/s Data Rate.
- The maximum number of re-timers is not expected to change from 2 to support the 32.0 GT/s Data Rate.

Changes will be made for the material associated with the following areas.

- The 32.0 GT/s Data Rate will be backwards compatible with the prior Data Rates. Thus, the Link will train to L0 in 2.5 GT/s and then move to the higher Data Rate(s). The TS1 and TS2 Ordered Sets in 8b/10b encoding as well as 128b/130b encoding will be enhanced to include the 32.0 GT/s Data Rate support (Symbol 4, Bit 5).
- The equalization flows will be similar to the 8.0 GT/s and 16.0 GT/s Data Rate equalization flows. After training to L0 in 2.5 GT/s, the Link will perform equalization at 8.0 GT/s, followed by 16.0 GT/s equalization, followed by equalization at 32.0 GT/s. Optimizing the Link to skip (or reorder) equalization at lower Data Rates when supporting 32.0 GT/s Data Rate is under discussion.

- The ElEOS Ordered set in 128b/130b encoding may be modified to include longer run length of 0s and 1s (e.g., alternate between 32 0b and 32 1b) if our analysis shows that the 16.0 GT/s EIEOS does not meet the electrical idle exit requirements at 32.0 GT/s Data Rate.
- The compliance patterns are expected to be identical to the 16.0 GT/s Data Rate, subject to analysis of the pattern at 32.0 GT/s Data rate. At 32.0 GT/s, another 19 sets of patterns with various presets will be added, similar to the 19 sets of patterns that were added for 16.0 GT/s Data Rate.

Aside from the above, no other changes are anticipated for the material in this chapter.

Chapter 5 – Power Management

No changes are anticipated for the material in this chapter.

Chapter 6 – System Architecture

No changes are anticipated for the material associated with the following areas.

- Software requirements to first Configuration Space access, Completion Timeouts

Chapter 7 – Software Initialization and Configuration

Aside from the following, no other changes are anticipated for the material in this chapter.

- We are expecting to have a new "Physical Layer 32.0 GT/s Extended Capability" structure for the 32.0 GT/s Data Rate.
- Reserved encodings in several register fields will be defined to accommodate the 32.0 GT/s Data Rate.

Chapter 8 – Electrical Sub-Block

A fifth generation data rate is added. It is 32.0 GT/s NRZ.

The maximum pad to pad loss target is expected to be approximately 35 dB

No changes are anticipated for the material associated with the following areas.

- The raw BER target remains 1.0 E-12
- The current number of Tx EQ taps and coefficient range is expected to be sufficient
- The current Tx EQ presets are expected to be sufficient
- The high-level channel compliance methodology with reference receiver and eye target is expected to be sufficient
    - Additional constraints such as insertion loss deviation and/or cross-talk magnitude may be considered
- Backward compatibility with all slower speeds is still required
- Tx voltage parameters remain unchanged

- The Tx and Rx stressed eye high level measurement methodologies will remain unchanged. However, the details will change.
- AC coupling cap requirements remain unchanged
- Transmitter and Receiver termination requirements remain unchanged
- Reference clock voltage specifications are expected to be sufficient, with the possible exception of maximum slew rate.

Aside from the above areas, a significant amount of the material for most of the areas in chapter 8 are expected to require changes to accommodate the 32.0 GT/s data rate.

Chapter 9 – Single Root I/O Virtualization and Sharing

No changes are anticipated for the material in this chapter.

Chapter 10 – ATS Specification

No changes are anticipated for the material in this chapter.

Appendices

No changes are anticipated for the material in the appendices.